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PTO/SB/21 (02-04)

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Total Number of Pages in This Submission

Application Number	10/686,318
Filing Date	October 15, 2003
First Named Inventor	Ware
Art Unit	2818
Examiner Name	
Attorney Docket Number	RAMB-01042US1

ENCLOSURES (Check all that apply)

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Kirk J. DeNiro, Esq., Vierra Magen Marcus Harmon & DeNiro LLP
Signature	
Date	July 14, 2004 7/14/04

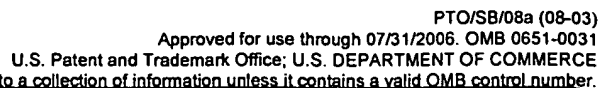
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Substitute for form 1449A/PTO

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Sheet	1
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of	2
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Application Number	10/686,318
Filing Date	October 15, 2003
First Named Inventor	Ware
Art Unit	2818
Examiner Name	Unknown
Attorney Docket Number	RAMB-01042US1

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Application Number	10/686,318
Filing Date	October 15, 2003
First Named Inventor	Ware et al.
Art Unit	2818
Examiner Name	Unknown
Attorney Docket Number	RAMB-01042US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ISHIBASHI et al., "A 300 MHz 4-Mb Wave-Pipeline CMOS SRAM Using a Multi-Phase PLL", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, pp. 1189-1195, November 1995	
		NAMBU et al., "A 0.65-ns, 72-kb ECL-CMOS RAM Macro for a 1-Mb SRAM", IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, pp. 491-499, April 1995	
		NAKAMURA et al., "A 220-MHz Pipelined 16-Mb BiCMOS SRAM with PLL Proportional Self-Timing Generator", IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, pp. 1317-1322, November 1994	
		YAMASHITA et al., "A 3.84 GIPS Integrated Memory Array Processor with 64 Processing Elements and a 2-Mb SRAM", IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, pp. 1336-1343, November 1994	
		ISHIBASHI, et al., "FP 18.5: A 300 MHz 4-Mb Wave-Pipeline CMOS SRAM Using a Multi-Phase PLL", IEEE International Solid-State Circuits Conference, pp. 308-309, February 1995	
		TAN et al., "FA 15.1: An 800MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.89m CMOS", IEEE International Solid-State Circuits Conference, pp. 258-259, February 1995	
		YAMASHITA et al., "FA 15.2: A 3.84 GIPS Integrated Memory Array Processor LSI with 64 Processing Elements and 2-Mb SRAM", IEEE International Solid-State Circuit Conference, pp. 260-261, February 1994	

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